UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,946	06/08/2004	H. Bernhard Pogge	FIS920020007US2	3945

32074 7590 02/28/2006

INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
BLDG. 300-482
2070 ROUTE 52
HOPEWELL JUNCTION, NY 12533

EXAMINER	
NGUYEN, DILINH P	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,946	POGGE ET AL.	
	Examiner	Art Unit	
	DiLinh Nguyen	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-26* is/are pending in the application.

4a) Of the above claim(s) *26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election of Embodiment 2, figs. 6A-6F and claims 21-26 in the reply filed on 12/2/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Remark

Applicant's election without traverse of Embodiment 2, figs. 6A-6F (claims 21-26) is acknowledged. However, claim 26 is directed to a non-elected invention (Embodiment 1, figs. 2A-5). Therefore, claim 26 is withdrawn from consideration as being directed to a non-elected invention.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 21-22 and 24-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Baba (U.S. Pat. 6369443) (newly cited).

Baba discloses an integrated structure including a semiconductor device and connector structures for connecting the semiconductor device to a motherboard, the integrated structure comprising:

a first layer 1 having a first set of conductors disposed therein, the first layer having an upper surface and a lower surface, the first set of conductors connecting to bonding pads disposed on the lower surface, the bonding pads being spaced with respect to each other with a first spacing distance in accordance with a required spacing of connections to the motherboard 16;

the semiconductor device 2;

a second layer disposed on the semiconductor device and in contact therewith, the second layer having a second set of conductors disposed therein connecting to the semiconductor device, the second layer facing the first layer;

a plurality of connectors 3 connecting the first set of conductors to the second set of conductors, said connectors being one of (1) a set of stud/via connectors and (2) a set of C4 connectors, said connectors being spaced with respect to each other with a second spacing distance less than the first spacing distance;

a support structure 7 attached to the upper surface of the first layer and in contact therewith and surrounding the semiconductor device, a gap between said support structure and the semiconductor device being filled with a fill material 4; and

connector structures 9 connected to the bonding pads 7 (fig. 7).

- Regarding claim 22, Baba discloses that the connector structures 9 form one of a ball grid array (BGA), a C4 array and a land grid array (LGA) (fig. 7).

- Regarding claim 24, Baba discloses that the support structure has an area corresponding to an area occupied by the bonding pads (fig. 7).

- Regarding claim 25, Baba discloses that the plurality of connectors 3 are a set of C4 connectors, and the fill material 4 fills a gap between the semiconductor device 2 and the first layer surrounding said C4 connectors (fig. 7).

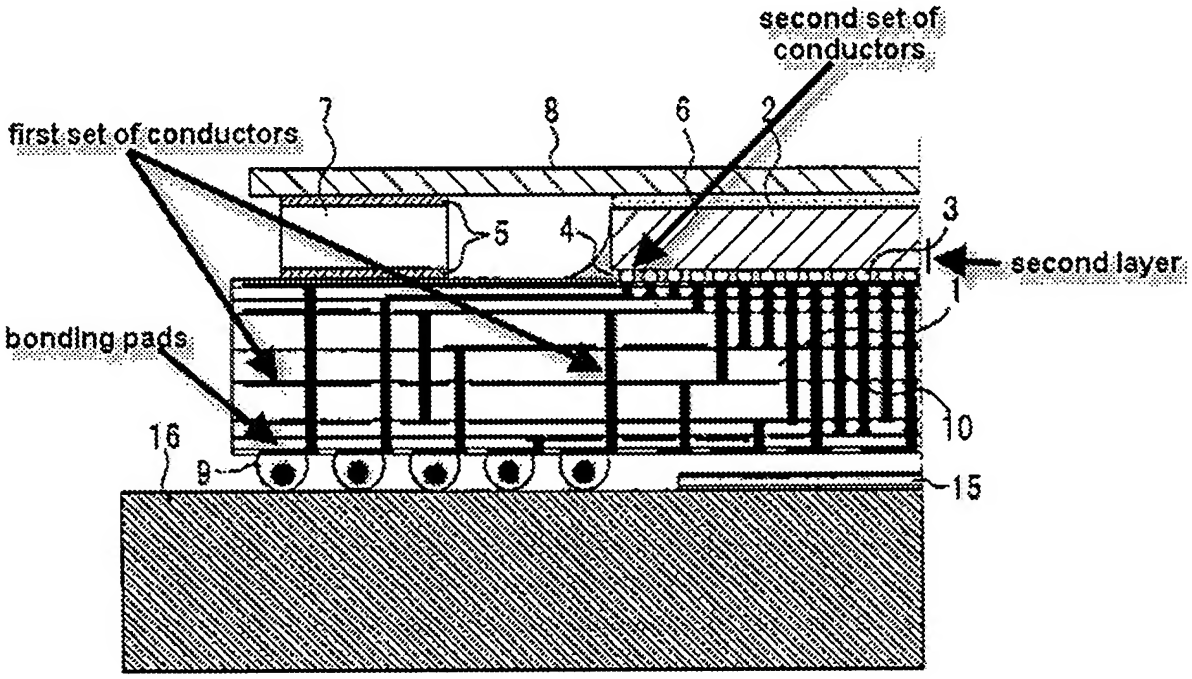

Fig. 7

3. Claims 21-22 and 24-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Honda (U.S. Pat. 6696764) (newly cited).

Honda discloses an integrated structure including a semiconductor device and connector structures for connecting the semiconductor device to a motherboard, the integrated structure comprising:

a first layer having a first set of conductors disposed therein, the first layer having an upper surface and a lower surface, the first set of conductors connecting to bonding pads 7 disposed on the lower surface, the bonding pads being spaced with respect to each other with a first spacing distance in accordance with a required spacing of connections to the motherboard;

the semiconductor device 13;

a second layer disposed on the semiconductor device and in contact therewith, the second layer having a second set of conductors disposed therein connecting to the semiconductor device, the second layer facing the first layer;

a plurality of connectors connecting the first set of conductors to the second set of conductors, said connectors being one of (1) a set of stud/via connectors and (2) a set of C4 connectors, said connectors being spaced with respect to each other with a second spacing distance less than the first spacing distance;

a support structure attached to the upper surface of the first layer and in contact therewith and surrounding the semiconductor device, a gap between said support structure and the semiconductor device being filled with a fill material 15; and

connector structures 15 connected to the bonding pads 7 (figs. 9C and 10).

- Regarding claim 22, Honda discloses that the connector structures 15 form one of a ball grid array (BGA), a C4 array and a land grid array (LGA) (fig. 9C).
- Regarding claim 24, Honda discloses that the support structure has an area corresponding to an area occupied by the bonding pads 7 (fig. 9C).
- Regarding claim 25, Honda discloses that the plurality of connectors are a set of

C4 connectors, and the fill material 15 fills a gap between the semiconductor device 13 and the first layer surrounding said C4 connectors (fig. 9C).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Honda (U.S. Pat. 6696764) (newly cited) or Baba (U.S. Pat. 6369443) (newly cited) in view of Dordi (U.S. Pat. 5835355) (previously applied).

Honda or Baba substantially disclose all the limitations as claimed above except for the support structure is provided with a TCE approximately that of the motherboard.

However, Dordi discloses a semiconductor device comprising a motherboard 32 is characterized by a thermal coefficient of expansion (TCE), and the support structure 34 is provided with a TCE approximately that of the motherboard (fig. 1, column 5, lines 7-10). Therefore, it would have been obvious to one having ordinary in the art at the time the invention was made to modify the device structure of Honda or Baba by having the support structure is provided with a TCE approximately that of the motherboard because as taught by Dordi, such the thermal coefficient of expansion would minimize thermal stress on the package and assembly during thermal cycling (column 2, lines 42-45).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (571) 272-1712. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DLN

HOAI PHAM
PRIMARY EXAMINER